AMENDMENTS TO THE SPECIFICATION

On page 1, please replace line 3 with the following amended line:

(MBHB Case No. 01-1205-A; Rambus Case No. RA238)

On page 3, at line 1 before the heading "**FIELD OF THE INVENTION**", please insert the following paragraph:

--**CROSS REFERENCE TO RELATED APPLICATIONS**

This is a continuation of U.S. Patent Application No. 10/112,963, filed on March 29, 2002, now U.S. Patent No. _____. The entire disclosure of U.S. Patent Application No. 10/112,963 is herein incorporated by reference.--

Please replace the paragraph on page 18, lines 3-15 with the following amended paragraph:

The value of the TEST signal is checked at step 256 to determine if the TEST signal has transitioned from logic one to logic zero. If the TEST signal is at logic zero, then the midpoint may have not been reached, and the control flow branches to step 262, where the value of X is incremented. The control flow then branches back to step 254 where a new set of control signals is generated based on the incremented value of X. The value of the TEST signal is again verified at step 256. If the TEST signal has transitioned to ~~the~~ a logic ~~zero~~one, ~~then the~~ control flow then branches, at step 260, to step 264~~,~~ where the value of X is decremented. The value of X is decremented because the transition to logic ~~zero~~ one indicates that the midpoint has been passed and the value of X is decremented, in this embodiment, to obtain a more accurate midpoint value. The value of X is now set for operation, and the QUP and QDOWN signals are generated. As

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mentioned in the preceding paragraphs, instead of setting the value of X to a minimum value, the value of X may be set to a maximum value and then decremented until the transition is detected.

Please replace the paragraph starting on page 20, lines 14 and continuing onto page 21, line 6 with the following amended paragraph:

FIG. 9 is a control flow diagram illustrating an embodiment of a process 370 performed by control circuit 340 for determining the value of n and setting the POWER CONTROL signal. Process 372 is similar to process 180 of FIG. 3. At step 372 (step 182 in FIG. 3) of process 370, the control circuit 340 initializes the value of n, and the POWER CONTROL signal is initialized such that all elements of delay lines 310 and 320 are active. At step 374 (step 184 in FIG. 3), the delay CONTROL signal is generated that drives the MUXes 112 and 122 of the delay circuit 300 to select the output taps from the delay lines 310 and 320. At step 376 (step 186 in FIG. 3), the output from a phase detector is checked to determine whether the phase of the FBCLK signal lags or leads the phase of the INPUT CLK signal. If the circuit 300 has not locked to the INPUT CLK signal, then control flow branches at step 380 to step ~~188~~378, where the control circuit 340 adjusts the value of n according to the signal output by the phase detector 142 and the control flow returns to step ~~384~~374 where the delay CONTROL signal is generated using the new value of n.

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